REMARKS/ARGUMENTS

Claims 1-18, 21-29, and 37 are pending. Claims 1-4, 7-18, and 25-26 are rejected under 35 USC 103(a) as being unpatentable over Kohda et al. (USPN 5,021,999) in view of Tigelaar (USPN 5,273,926). Claims 5, 6, 21-24, 27-29, and 37 are rejected under 35 USC 103(a) as being unpatentable over Kohda et al. in view of Tigelaar and Guterman (USPN 5,153,691). These rejections are respectfully traversed.

In the present Office action, the Examiner maintains the same rejections based on the same references and same arguments set forth in the prior Office action mailed on January 23, 2003. However, in response to Applicants' arguments set forth in the amendment filed on May 23, 2003, the Examiner in paragraph 3 of the present Office action states:

> Regarding applicant's arguments on page 2, second paragraph that the patent draftee of the Tigelaar et al. patent mistakenly matched up control gates 90 in FIG. 5e with column lines 16 in Fig. 1 instead of with row lines 12, and conversely mistakenly matched up source and drain regions with row lines 12 instead of column lines 16, the Examiner respectfully disagrees. The applicant has not shown any evidence of why this is a drafting error except stating "It is notoriously well known in this art that in semiconductor memory arrays, gates of memory cells form row lines which are coupled to a row decoder, and drain and source regions of memory cells form column lines which are coupled to a column decoder." Therefore the statement carries no weight. However even if this statement were true, row lines and column lines are functionally and structurally identical to each other that it would make no difference whether the control gates were matched with either row lines and column lines.

As set forth below, Tigelaar not only provides the evidence supporting the Applicants' assertion that the statement in column 5, lines 33-36 of Tigelaar is incorrect, but also serves to highlight the flaw in the Examiner's assertion that "row lines and column lines are functionally and structurally identical to each other."

The statement at column 5 lines 33-36 of Tigelaar which includes the drafting error is:

> Control gates 90 as shown in Fig. 5e correspond to the column lines 16 shown in Fig. 1, while the source and drain regions 74 and 76 correspond to the row lines 12.

That this statement is erroneous is clearly evident from Tigelaar's disclosure. First, Tigelaar in column 3 lines 62-66 states:

> A resist pattern 55 is then used as shown in FIG. 3b to form elongated strips of heavily doped N+ regions that run the length of the array and form the source and drain bit lines.

Emphasis is added. Here, Tigelaar sets forth the processing step for forming source regions 74 and drain regions 76. Tigelaar makes clear that the N+ source and drain regions run the length of the array to form source and drain bitlines. Bitlines form the array column lines. Thus, the above statement (in column 3, lines 62-66) of Tigelaar makes clear that source region 74 and drain region 76 correspond to column lines 16 in FIG. 1, not "the row lines 12" as stated in column 5, lines 34-35 of Tigelaar.

Second, Tigelaar in column 4, lines 54-56 states:

> The poly is then patterned and etched perpendicular to the source and drain bit lines to form the wordlines 90 as shown in FIG. 5c.

Emphasis is added. Here, Tigelaar describes the processing step for forming wordlines 90 which are also referred to as control gates 90 (see e.g., column 5, lines 25-26). Wordlines form the array row lines. Thus, Tigelaar's characterization of control gates 90 as "wordlines" makes clear that contrl gates 90 correspond to the row lines 12 in FIG. 1 not "column lines 16" as stated in column 5, lines 33-34 of Tigelaar.

The above-cited statements of Tigelaar not only support the Applicants' contention that Tigelaar's statement in column 5 lines 33-35 erroneously matches up the control gates and bitlines in FIG. 5c with row lines and column lines in FIG. 1, but also highlights the Examiner's flawed assertion that "even if this statement were true, row lines and column lines are functionally and structurally identical to each other that it would make no difference whether the control gates were matched with either row lines and column lines."

As mentioned by Tigelaar, bitlines or column lines are made of N+ diffusion regions and are coupled to the cell drain and source regions, while wordlines or row lines are made of polysilicon and are coupled to the cell control gate. The drain and source regions serve a completely different function than the control gate during read, erase, and program operation. Thus, contrary to the Examiner's assertion, row lines and column lines are neither structurally nor functionally similar let alone "identical." Should the Examiner maintain his assertion that

"row lines and column lines are structurally identical," the Applicants respectfully request that the Examiner provide support for this assertion.

As support for Applicants' assertion that it is notoriously well-known in the semiconductor memory technology that the gates of memory cells along each row form row lines and the source and drain regions of a the cells along each column form the column lines, Applicants provide the attached document. The attached document includes relevant pages of the text book titled "SEMICONDUCTOR MEMORIES", second edition, by Betty Prince. Figures 11.13, 11.27, and 11.37 clearly show that the gates of memory cells along each row form wordlines or row lines, and the source and drain regions of memory cells along each column form bitlines or column lines.

In paragraph 5 of the Office action, in response to the Applicants' prior arguments, the Examiner states:

> Regarding the applicat;s argument on page 3, middle paragraph that extending control gate 6 over drain and source regins 2, 3 prevents column lines from contacting the drain and source regions, the Examiner respectfully disagrees. Tigelaar shows (see FIG. 3e) control gates 90 that extend over drain and source rgions 74, 76 without contacting the drain and source regions.

The Examiner clearly misunderstands the argument by the Applicants. The Applicants agree with the Examiner Tigelaar shows that control gates 90 extend over drain and source regions. However, Applicants argue that applying this teaching to Kohda renders Kohda unsatisfactory for its intended purpose. More specifically, in Kohda, extending control gate 6 over drain and source regions 2, 3, as taught by Tigelaar, prevents column lines (bitlines) from contacting the drain and source regions. Kohda extends control gate 6 vertically, in part, to make surface areas of the drain and source regions exposed so that column lines can make contact with the drain and source regions. This is more clearly shown in Fig. 7 wherein Kohda uses bitlines BL1-BL5 to make contact to a common source region and common drain region between every two adjacent cells along each row of cells. If control gate 6 was extended horizontally to cover the source and drain regions as suggested by the Examiner, contact could not be made to the source and drain regions. This not only prevents supplying the proper biasing to program, erase, or read the cell, but also prevents forming the particular array architecture shown in Fig. 7.

Kohda achieves its primary goal of storing tri-level data (see Title, Abstract, and Field of the Invention) by incorporating the cell in Figs. 3A, 3B in the specific array architecture shown in Fig. 7. This array architecture is designed to supply the requisite biasing to the array for storing tri-level data in the memory cells. By eliminating the ability to directly contact the common source and common drain regions with the bitlines, the required biasing for storing tri-level data can not be provided to the cells. Th erefore, modifying the cell as suggested by the Examiner renders Kohda's cell unsatisfactory for its intended purpose of storing tri-level data.

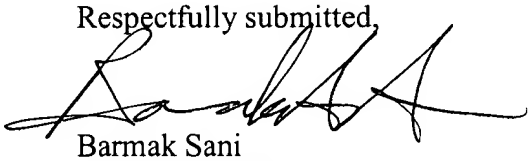
Thus, Applicants believe that each of claims 1 and 28 and their respective dependent claims distinguish over Kohda and Tigelaar et al. taken singly or in combination at least for the reasons set forth herein and in the previous amendment filed on May 23, 2003.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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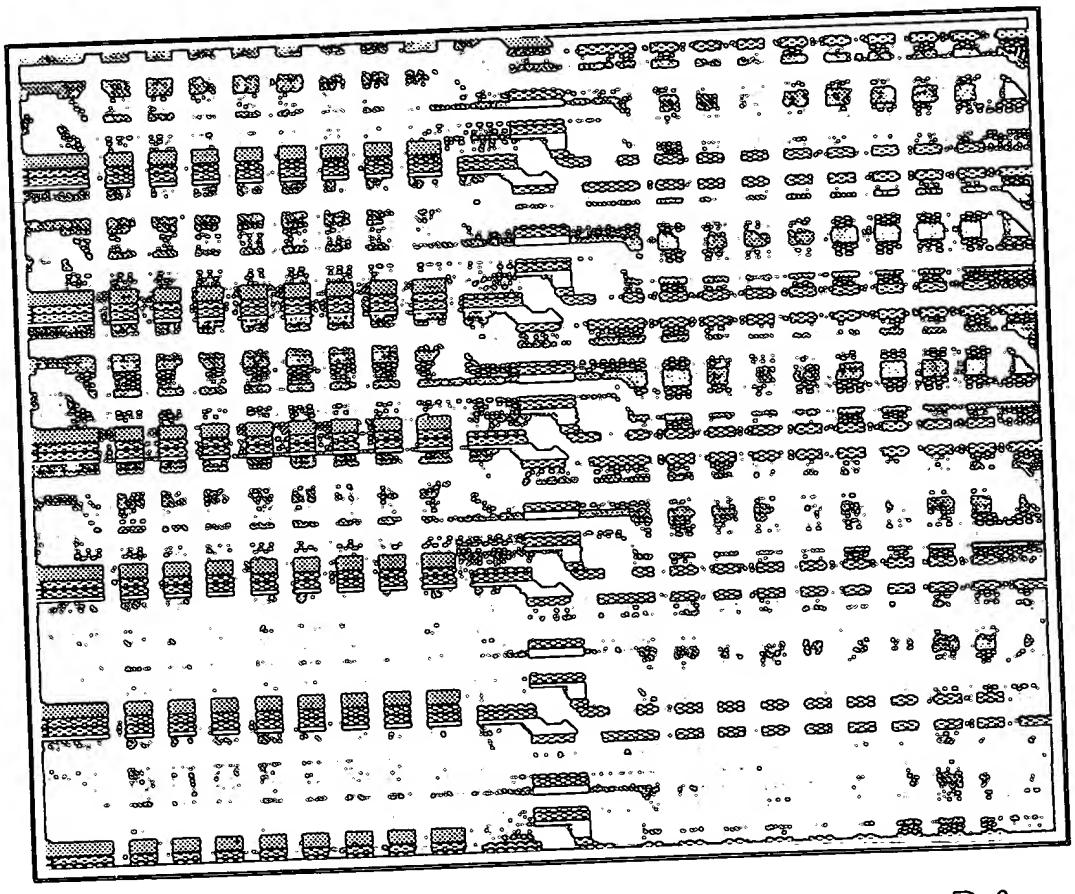

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A Handbook of Design, Manufacture and Application

Second Edition

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clock cycle. For this reason non-coincident address transitions did not cause the circuit to malfunction.

A clocked row decoder circuit used in this chip had zero static current consumption. Power was dissipated in the selected decoder only during the brief time after an address transition when the row clock was low. A conventional static sense amplifier circuit which drew dc current during sensing is shown in Figure 11.12(a) compared to the clocked sense amplifier circuit used in this 64k EPROM which is shown in Figure 11.12(b). The use of the dynamic sense amplifier greatly reduced the power consumption.

This was also one of the first of the EPROMs to incorporate special test features into the circuit to reduce test time. Another CMOS EPROM which featured on-chip test circuits was a 256k from Toshiba [40] shown in 1985. Typically testing is very time consuming for EPROMs constituting a major component of production cost. These ease-of-test features are considered at more length in the chapter on memory testing.

11.4 HIGH SPEED CMOS EPROMs

11.4.1 ATD for speed

An example of using address transition detection for improving access time was shown in a Toshiba [44] 80 ns 1Mb CMOS EPROM in 1985. In this chip a precharge pulse was used to minimize the bit-line and sense line delays. The precharge pulse was initiated from the ATD circuit and terminated by a delayed pulse through a dummy word-line. Only the selected bit-line was precharged to minimize peak current during the precharge cycle. The sense line was also equalized to a reference level. A type of divided word-line structure was used dividing the array into four blocks to reduce the word-line delay. A two-stage sense amplifier was used with a high sensitivity preamplifier which was sensitive to small voltage differentials. This minimized the required bit-line swing.

The ATD was used also to provide an automatic power-down function with the chip being automatically disabled by an internal pulse 360 ns after chip activation.

Another chip which used ATD to improve access time was an Intel 256k EPROM introduced in 1985. This part was particularly notable for its 'unerasable EPROM (UPROM)' cells which will be covered in the chapter on yield and redundancy.

Two other 1Mb EPROMs used ATD to improve speed, an 80 ns part from Fujitsu [48] and a 70 ns part from STM [49]. The STM chip used four techniques for enhanced speed. The memory array was divided into four quadrants to reduce the bit-line capacitance. The row decoder was interleaved. This helped improve performance since normally the very small pitches between cells in EPROMs require very simple row decoders that are not optimized for speed. By interleaving the row decoders SGS-T had the space of two cell pitches in which to fit an optimized row decoder. Address transition detection from column address was used for the bit-line precharge and equalization.

A fast 1Mb 55 ns part was shown by Hitachi [50]. This 64k × 16 chip used tungsten polycide to reduce word-line delay. It was shown that a single sense amplifier, in this case of a 16 bit wide EPROM, was faster than the delay through several staged sense amplifiers. Ground bounce was reduced by a special output buffer arrangement resulting in less delay in the output buffers and hence faster read operation.

11.4.2 Double-layer metal strapping for speed

A fast 23 ns 256k EPROM from Cypress [51] in 1989 used a double-layer metal technology to strap word lines in the array and to bus signals in the periphery. Bit-line length was reduced to 256 cells. In addition, speed was enhanced by the use of differential sensing, address transition detection and a ground switched decoding scheme. The address transition detection circuits were divided between the top and bottom of the chip to reduce the parasitic capacitance. These signals merged to form a composite signal that triggered the equalization signal. The outputs were latched during address transition to improve noise immunity.

Another very fast part, a 16 ns 1Mb EPROM from Toshiba [72] shown in 1990, also used double-layer metal technology to strap word-lines in the array to enhance speed. The cell array was divided into eight sections to reduce bit-line capacitance. The word-line delay was reduced by a double word-line structure similar to that used in the static RAMs. The row main decoder used a feedback circuit to guarantee high speed without reducing voltage. The section word-line was selected using a NOR gate whose inputs were a second aluminum main word-line and one of the section selection lines. The section word-lines in non-selected sections were set low to save power. The section word-line was made of MoSi to reduce delay. A three-stage differential sense amplifier scheme was used. Complementary nodes in the sense amplifier were equalized by an ATD pulse to speed sensing.

11.4.3 New transistor structures for speed

One approach to enhancing read access time and programming time was a high read current split gate cell developed by Waferscale Integration [52] in 1987. The cross-section of this cell is shown in Figure 11.13(a) and the equivalent circuit in Figure 11.13(b). The cell was comprised of a MOS transistor in series with a floating gate transistor merged into a single composite device which was essentially a 1.5-transistor cell.

The cell had a high read current of over 150 μA which provided access times as low as 35 ns and a fast programming rate of less than 1 ms. The programming mechanism of the split gate EPROM cell was channel hot-electron injection. The fast programming rate was due to the short channel length of the floating gate transistor.

A two-transistor cell high speed 16k CMOS EPROM was introduced to the market by TI [70] in 1987. The two transistors were used for differential sensing. Because of the differential cell the sense amplifier could detect a programmed or unprogrammed state with a smaller voltage swing which implied a faster access time.

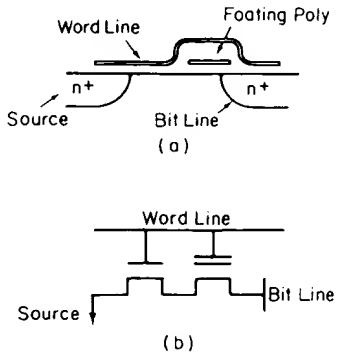

Figure 11.13
Schematic cross-section (a) and equivalent circuit diagram (b) of a high read current split gate cell with the select transistor integrated in series with the floating gate transistor. (From Ali *et al.* [52], Waferscale Integration 1988, with permission of IEEE.)

The differential sensing scheme also meant that the outputs of the unprogrammed EPROM were in an indeterminate state which can be sensed without programming by using a 'blank check' mode which will be described in the section of Chapter 14 on EPROM programming. This eased the test difficulties of one-time-programmable EPROMs. The drawback was that both the logic '0' and the logic '1' states need to be programmed.

Another two-transistor cell for high speed EPROMs was developed by Cypress [70]. This cell had separate read and program transistors with the floating gates connected. It used a single-ended sensing scheme. The sense amplifier used a reference voltage on one input and the read transistor on the other. This single-ended sensing had the effect of causing an erased device to contain all '0'.

For lower density high speed EPROMs, Cypress [68, 69] used a four-transistor differential memory cell. This cell was optimized for high read current and fast programmability. This was accomplished by separating the read and program transistors as shown in Figure 11.14(a). The program transistor had a separate implant to maximize the generation and collection of hot electrons while the read transistor implant dose was chosen to provide a large read current. The problem of injecting unwanted charge onto the floating gate during the read operation was eliminated since the read and program transistors were separate and the program transistor drain could be grounded during the read operation.

The two sets of read and program transistors were used for differential sensing with a three-stage sense amplifier which is shown in Figure 11.14(b). The read and program paths were separated to optimize speed. The X and Y decoding paths were predecoded to optimize the power delay product.

These fast EPROMs could be used in 'zero wait state' systems with high performance microprocessors. An example of this requirement for various processor clock frequencies [70] is shown in Table 11.5.

These lower density high speed EPROMs competed with bipolar PROMs in applications such as control stored in bit-slice based designs and in statemachine

Table 11.7 Technological characteristics of early CMOS EPROMS 4Mb–16Mb.

Date	Company	Density	Channel (μm)	Cell (μm^2)	Chip (mm^2)	Gateox (nm)	Interox (nm)
1987	Toshiba	4Mb	0.9	9.0	87.4	20	30
1988	Intel	4Mb	1.0	11.9	83.4	25	28
1989	Toshiba	4Mb	0.9	9.0	86.0	20	30
1990	Hitachi	4Mb	0.8	7.8	75.3		
1990	NEC	16Mb	0.9	3.6	121.4	20	20

Table 11.8 Electrical characteristics of early CMOS EPROMS 4Mb–16Mb. (Source 1987–1990 ISSCC Proceedings.)

Date	Company	Density	Org	V_{PP} (V)	T_{PP} (s)	I_{AC} (MHz) (mW)	I_{SB} (μW)	t_{ACS} (25) (ns)
1987	Toshiba	4Mb	512k × 8	12.5		5(1)	0.05	120
1988	Intel	4Mb	256k × 16	12.5	3	100(1)	50	90
1989	Toshiba	4Mb	512k × 8	12.5	1			68
1990	Hitachi	4Mb	256k × 16	12.5	1			55
1990	NEC	16Mb	2Mb × 8/1Mb × 16	12.5	10	18(8.3)	5.0	85

Technological and electrical characteristics of 4Mb to 16Mb EPROMs are shown in Tables 11.7 and 11.8.

11.10.1 Innovative cell developments for 4Mb EPROMs

Both new process technologies and innovative cell structures were considered in the course of developing the tiny 6 to 7 μm^2 cells required for cost effective 4Mb EPROMs.

One of the first 4Mb EPROMs, shown in 1987 by Toshiba [55, 57], used the 9.0 μm^2 cell shown in Figure 11.27(a). Relatively tight 0.9 μm design rules, obtained with advanced stepper lithography, were used along with RIE. Programming was by channel hot election injection to the floating gate.

This cell used some of the most advanced manufacturing techniques available on the conventional cell technology. It used LOCOS to isolate individual bits, and a half contact per cell to connect drain diffusions to the metal bit lines. Even with a self aligned contact and self aligned floating gate, there were still alignment tolerances involved which tended to limit the reduction in cell size.

Hitachi [59] managed, using scaling to 0.8 μm minimum geometries with similar conventional but highly sophisticated processing techniques, to create an even smaller 7.8 μm^2 cell.

The process was becoming very expensive and sophisticated. It was time for some innovation in the basic cell structure and technology.

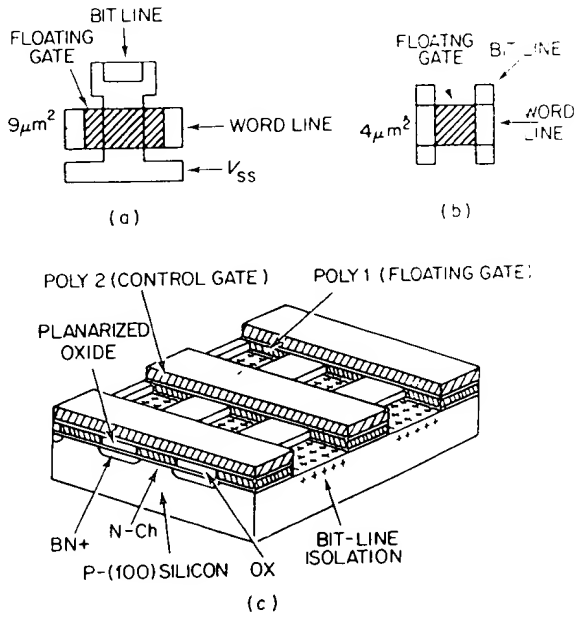

Figure 11.27
Early 4Mb EPROM cell structures. (a) 9.0 μm^2 conventional cell in 1.0 μm design rules. (b) 4.0 mm^2 cross-point cell in 1.0 μm design rules. (c) Three-dimensional diagram of EPROM array using cell shown in (b). (From Mitchell *et al.* [53], TI 1987, with permission of IEEE.)

Two innovative cell structures for 4Mb EPROMs were shown by Texas Instruments [53] and Toshiba [54] the same year. The TI cell used clever process techniques to make a true cross-point EPROM cell. The Toshiba cell used clever NAND gate cell architecture. The TI [53] cell, shown in Figure 11.27(b), did not require use of LOCOS isolation or contacts in the array, and was fully self aligned. Only masking levels, bit-line and word-line, were needed for fabrication of the cell. The cell was about half the size of the conventional cell using the same 1.0 μm design rules.

A three-dimensional schematic diagram of an EPROM array using this cell is shown in Figure 11.27(c). The stacking of the poly 1 interspersed with oxide and the poly 2 in the direction of the poly 2 bit-lines was achieved by a planarization process which leveled the poly 1 and oxide before deposition of the poly 2. A schematic representation of this fabrication process is shown in Figure 11.28.

The Toshiba [54] cell changed from the normal NOR structure used in EPROMs to a NAND structure such as described previously in the ROM chapter. A comparison between the Toshiba NAND cell and the conventional EPROM cell is shown in Figures 11.29(a) and (b). An equivalent circuit of the NAND structure cell with 4 bits is shown in Figure 11.29(c). The new cell is only about 70% of the size of the conventional cell in the same 1.0 μm design rules.

The NAND structure cell can be programmed by hot electron injection to the floating gate and be erased by either UV irradiation or by electric field emission of

ques including divided bit-lines, a symmetric sense amplifier configuration and a chip-enable transition detector to improve stable data sensing and provide high speed access time.

Output noise reduces the TTL input noise margin and can cause erroneous addresses to be read. It also can effect the data sensing circuitry, particularly in EPROMs with a single-ended sensing scheme, as described in Chapter 5, and cause erroneous data to be read.

Large current flows in the data-out buffers due to temporarily incorrect data are one source of internal noise in an EPROM. Figure 11.34(a) shows a sense line and bit-line structure. Figure 11.34(b) shows the potential changes by the Y_0 and Y_1 column select signals along with the waveforms of the selected bit-line, sense line and data out on the selected bit-line. When a programmed cell in bit-line BL_1 is selected, the bit-line is charged to $V_{bias}-V_{thres}$. The sense line potential is raised higher than the reference line level and the data out are low level.

Next, the column address changes and a programmed cell on the discharged bit-line BL_2 is selected causing the sense line level to drop instantly pulled down by the low bit-line level. As the bit-line gradually charges, the sense line comes up so that even if the cell's data are '0', data out changes temporarily from '0' to '1', then back to '0' as the sense-line level exceeds the reference level. A similar waveform occurs when the $\overline{CE}$ signal activates the chip and data '0' is read out.

Another source of internal noise in an EPROM is the phase mismatch in single-ended sense circuitry which is due to the sense line and reference line not having the same structure. Many memory cell transistors are attached to the sense line but not to the reference line so the sense line has a significantly higher capacitance than the reference line. This means that when a voltage bump occurs the two lines oscillate at different frequencies and are hence out of phase; thus the sense line level surpasses the reference line level periodically causing incorrect data to be read out.

These noise sources were addressed in the 1989 Toshiba 4Mb EPROM by several methods. One was using a divided bit-line technique which decreased the bit-line charging time and permitted the cell to have a sufficient current read margin with a smaller cell read current. Another was to use a balanced sense amplifier with dummy bit-lines, as shown in Figure 11.34(c), so that the sense line and reference line oscillated in phase at the same frequency.

A 90 ns 4Mb EPROM from Intel [56] also took design measures against output noise sources which delayed chip speed. This part included a balanced sense amplifier and an output buffer circuit that ensured a mutually exclusive condition of the N-channel drives. In addition, the outputs were switched in succession rather than all at once to reduce the effective inductive dI/dT.

11.11 THE EARLY 16Mb CMOS EPROM CELL DEVELOPMENT AND DEVICES

Several companies described possible cells in the 0.6 μm geometry which appeared to be required for the sub 4 μm^2 cells required for the 16Mb EPROM. These included STM, Toshiba and NEC. An early 16Mb EPROM was shown by NEC in 1990.

STM [63] in 1989 presented a contactless cross-point cell with overlapping floating gate which was self aligned to the field oxide. The traditional 'T' cell is shown compared to the new cross-point cell in Figures 11.35(a) and (b).

The new cell forms a virtual ground array which is shown compared to a standard common ground array in Figures 11.35(c) and (d). This cell, like the TI cross-point cell mentioned earlier, used a planarization step after the stacked gate definition. This cell, however, maintained the use of field oxide.

In a separate paper STM [62] described the 16Mb EPROM process which featured less than 0.2 μm 'bird's beak' isolation, LDD N-channel and P-channel transistors, 20 nm interpoly dielectrics, and cold processing involving rapid thermal annealing. This produced a cell of the standard T-shaped type that was less than 4.5 μm^2 and presumably an even smaller cell of the new cross-point type. The soft write endurance for various geometry processes is shown in Figure 11.36.

Toshiba [64] also presented a virtual ground array cell for the 16Mb EPROM in 1988. This cell used an asymmetrical lightly doped source cell structure which is shown in Figure 11.37(a) along with a circuit schematic for the equivalent virtual ground array shown in Figure 11.37(b). They found that the asymmetrical cell had a higher immunity to the soft-write and write-disturb problems that appear to be

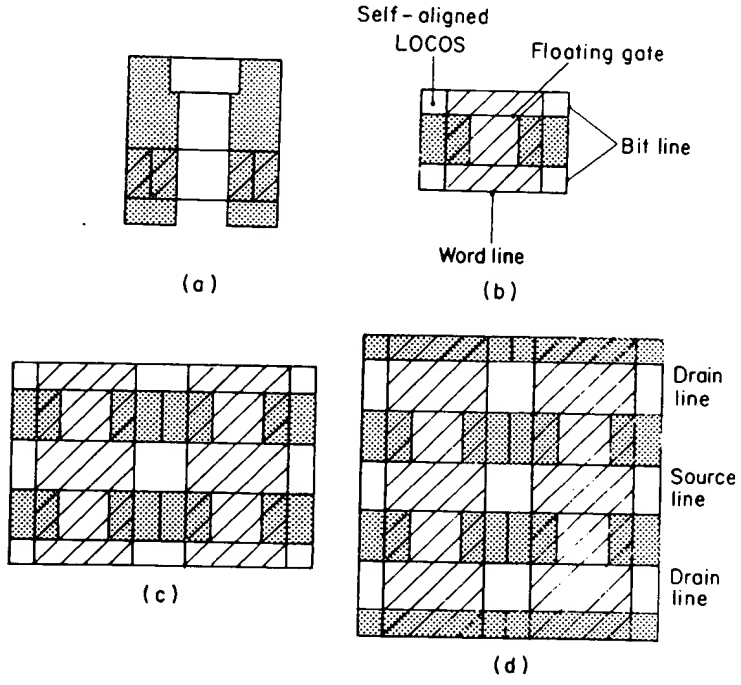

Figure 11.35
Layouts of cell structures for 16Mb EPROMs. (a) Traditional 'T' cell structure. (b) New cross-point cell structure. (c) Four of the cross-point cells in a 'virtual' ground array. (d) Four 'T' cells in a common ground array. (From Bellezza *et al.* [63], STM 1989, with permission of IEEE.)

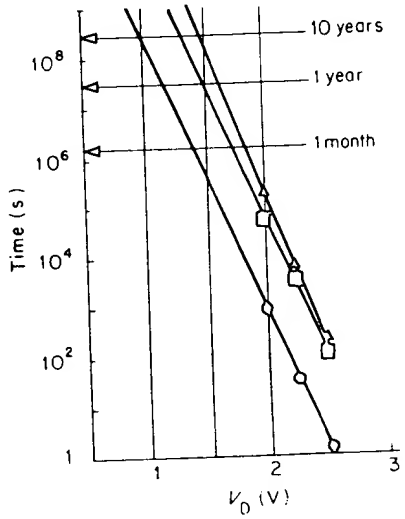

Figure 11.36
Soft write endurance for various geometries of 'T' type cell in a 16Mb process technology with ΔV_t of 200 mV and $V_{GS} = 5.5$ V. (○ $L_{drawn} = 0.4\ \mu m$, □ $L_{drawn} = 0.5\ \mu m$, △ $L_{drawn} = 0.6\ \mu m$). (From Bergemont *et al.* [62], STM 1989, with permission of IEEE.)

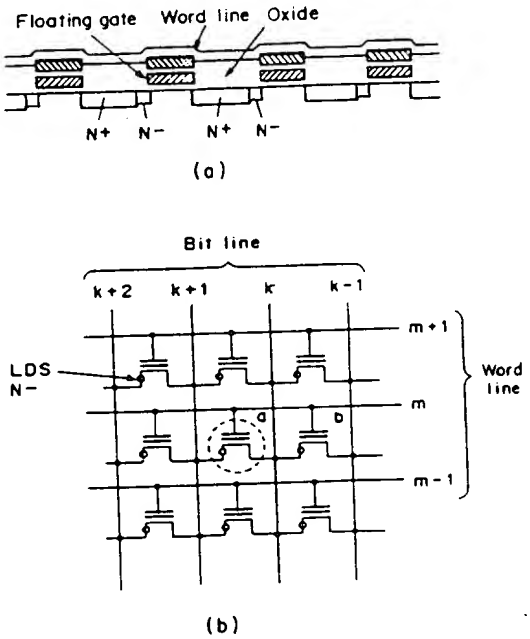

Figure 11.37
16Mb EPROM asymetric lightly doped source cell structure. (a) Schematic cross-section. (b) Circuit schematic for the virtual ground array formed by these cells. (From Yoshikawa *et al.* [64], Toshiba 1988, with permission of IEEE.)

associated with virtual ground designs. In 1990 Toshiba [99] showed an asymmetrical cell for the 16Mb CMOS EPROM in 0.6 μm technology. This cell, which is shown in Figure 11.37(c), was a modification of the earlier diffusion self-aligned cell used on the 4Mb EPROM. The multiple diffusions were accomplished with large tilt angle ion implantation of boron. This cell was also usable as a flash EPROM cell with minor modifications.

Another virtual ground EPROM architecture was described by Wafer Scale Integration [105] in 1991 for a 1Mb EPROM. This part improved speed by reducing the bit-line capacitance by using a segmented diffused bit-line scheme connected to a global metal bit-line. Address transition detection and a programmable signal development timer were also used.

Toshiba [65] in addition in 1989 investigated and proposed a new set of scaling rules for high density EPROMs as well as making modules of a scaled 3.85 μm^2 EPROM cell.

The scaling rules used, as prior constraints, the two required cell characteristics of reliability and performance. Independent scaling factors were introduced using 'k' for lateral dimensions and 'h' for vertical dimensions. An attempt was then made to empirically find a relation between k and h that satisfied both the reliability and performance constraints simultaneously. The results are shown in Figure 11.38.

Key issues which were considered included drain stress, gate stress, soft-write, cell read current, programming and punch-through.

Drain stress is a form of program disturb involving deprogramming of unselected cells on the same bit (drain) line as the selected cell. This was avoided by requiring that the electric field be maintained as in earlier generations of EPROMs. Since the field across the thin oxide (E_{ox1}) depends on the ratio of 'delta V_t/T_{ox1}', this requirement is that 'delta V' be scaled as $1/h$.

Gate stress is another form of program disturb involving deprogramming of an unselected cell on the same word line. Leakage through the interpoly dielectric is the main cause here and requires maintaining the electric field across the interpoly oxide. This translated to V_{PP} and V_t being scaled as $1/h$.

Soft write, which was discussed earlier, is a form of read disturb in which unselected cells are unintentionally written during the read operation. The reliability requirement of 10 years lifetime here required that V_{dr} be scaled for read disturb resistance.

One other interesting result of this study was that the programming voltage is optimized at V_{PP} below 5 V which could mean that the 16Mb EPROM will have internally generated V_{PP}.

Another process involved a 3.6 μm^2 16Mb EPROM cell which NEC [66, 67] showed in 1989 and used in 1990 in an early 16Mb EPROM. The technology included self-aligned trench isolation to reduce the spacing between the 3.6 μm^2 cells. Oxide–nitride–oxide (ONO) was used for the interpoly dielectric. A selectively deposited tungsten plug was used for the bit-line contact. While the gate length was 0.9 μm, the contacts used an 0.6 μm technology. A three-dimensional cross-section of the cell is shown in Figure 11.39(a) along with the top cell layout shown in Figure 11.39(b).

The 16Mb EPROM had a 121 mm^2 chip size which is right on the trend line shown